# AC Filterless Flexible LCC HVDC with Reduced Voltage Rating of Controllable Capacitors

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*DOI:*
10.1109/TPWRS.2018.2800666



*Document Version*
Peer reviewed version

*Citation for published version (Harvard):*
Xue, Y, Zhang, X & Yang, C 2018, 'AC Filterless Flexible LCC HVDC with Reduced Voltage Rating of Controllable Capacitors', *IEEE Transactions on Power Systems*. https://doi.org/10.1109/TPWRS.2018.2800666

# AC Filterless Flexible LCC HVDC with Reduced Voltage Rating of Controllable Capacitors

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***Abstract*—This paper presents a further significant development to the developed Flexible LCC HVDC system with controllable capacitors [1], which can provide AC voltage/reactive power control [2]. The development involves the installations of fixed parallel capacitors at the valve side of converter transformer, which brings the following significant benefits: 1) AC filter banks at the AC side of converter transformer are not needed as a better harmonic filtering performance can be achieved; 2) significant reduction of the HVDC station land requirement (compared with traditional LCC HVDC), as the AC filters together with the switchgear can occupy over 50% of the HVDC station footprint; 3) up to 50% reduction of the required voltage rating and more than 60% reduction of the capacitance of controllable capacitors for commutation failure elimination can be achieved while similar power system dynamic performance (AC voltage/reactive power control) compared with that in [1] can be demonstrated. Detailed analyses are presented to illustrate the effective commutation process and superb harmonic filtering performance. Selections of the component values are presented. Simulation results in RTDS are presented to verify the effectiveness of commutation failure elimination, power system dynamic performance, harmonic filtering performance and show voltage/current stress of the fixed parallel capacitors.**

***Index Terms*— HVDC, LCC HVDC, Flexible LCC HVDC, AC Filterless Flexible LCC HVDC, AC Filter, commutation failure, commutation failure elimination, controllable capacitor, energy storage, energy storage by capacitor, energy storage by controllable capacitor.**

## I. Introduction

For the problem of Commutation Failure (CF) in conventional Line Commutated Converter (LCC) based High Voltage Direct Current (HVDC) system, reference [1] proposed the LCC HVDC system with controllable capacitors to eliminate CF. The required voltage rating and capacitance of controllable capacitors are 140kV and 585μF. As the voltage rating directly determines the required number of power electronic switches (hence the associated costs and losses) and the capacitance is directly related to the physical size and cost of capacitor, it would be economically advantageous if both the voltage rating and the size of capacitor can be significantly reduced.

At the same time, from the power system dynamic point of view, it is important that these desired reductions are achieved not at the expense of deteriorated dynamic performance of the HVDC system, i.e. AC voltage/reactive power control [2].

Another operating characteristic of conventional LCC HVDC system apart from CF and reactive power consumption is that it generates considerable amount of AC harmonic currents [3]. Unless measures are taken to limit the amplitude of harmonics entering into the AC network, some of the following undesirable effects may occur: overheating of capacitors/generators and interference with telecommunication systems. Limits on acceptable harmonic distortion are normally defined by network operators or national legislation. Traditionally, the main methods of reducing the harmonic penetration into the AC system are a) increasing the pulse number and b) installation of passive AC filters.

A pulse number of 12 can be easily achieved with star-star and start-delta transformers connected in parallel and this configuration has been generally accepted for LCC HVDC [4]. For pulse number over 12, the implementation becomes uneconomical as it requires complex transformer connections and the consequent insulation of transformers becomes difficult [3]. As a result, harmonic reduction beyond the economic range of higher pulse configuration is achieved through the use of passive AC filters.

The design and implementation of passive AC filters are proven to be valid in meeting the corresponding harmonic limits over a long period of years for many HVDC schemes. However one of the significant drawbacks of passive AC filters in traditional LCC HVDC is their land requirement. These filters are physically large and together with the switchgear can occupy over 50% of the overall HVDC station footprint [5]. For example, a ±500kV 3000MW station requires a footprint of 240000m$^2$ [6]. It can be expected that the station footprint will continue to grow with the increased rating of LCC HVDC systems. This causes difficulty in the site selection of converter station especially when the available site area is restricted or prohibitively expensive [7]. In addition, AC harmonic filters are also responsible for up to around 10% of the total converter station losses [8] and around 9% of the converter station cost [9].

This work was sponsored by EPSRC Grant EP/L017725/1 and EP/N032888/1

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To develop more efficient filters, Continuously Tuned (ConTune) filters [10] and active filters [11-13] have been proposed. ConTune filter utilizes a static reactor with variable inductance to adjust the tuning frequency to follow the frequency and component variations [10]. As ConTune filters can be built to generate small amount of reactive power but still provide good filtering, they have been used for Capacitor Commutated Converter (CCC) based HVDC systems [14-16]. The additional cost incurred by providing the varying inductance need to be justified by the improved performance. Active AC filters are normally connected to the high-voltage system through a passive filter, forming the so-called hybrid filter [17]. This arrangement limits the rating of the active part and reduces the cost of the hybrid filter. However, traditional passive filters have still shown to provide the most technical and economical beneficial solutions [18].

In parallel with the development of more efficient AC filters, other methods have been proposed to reduce the filtering requirements by modifying the converter bridges or converter transformers [19-23]. The method of DC ripple reinjection was originally proposed in [19] and has been subjected to various developments over the years [20]. The idea is to increase the converter pulse number by reinjecting the current (derived from the ripple of DC voltage) into the secondary side of converter transformer. It requires modification of the converter bridges (by adding power electronic switches and reinjection transformers) and is not cost competitive compared with the use of filters. Alternative method for harmonic elimination using parallel delta-connected filtering windings for converter transformers is proposed in [23] which is a further development from the inductive filtering method from [21]. The traditional AC filters are still needed for both methods and triple-winding transformers need to be specially designed for the connection of filters. Therefore the size of AC filters is not significantly reduced and it leads to higher cost and complexity of the converter stations compared with the method proposed in this paper. A new three-winding transformer with negative leakage inductance is proposed in [22] to eliminate AC harmonics. However the method is only effective when a resistive load is connected to the output of inverter system.

From the above analysis, it would be attractive that if the harmonic filtering performance could be achieved with only passive components under simple arrangement. This would bring the advantages of 1) much less converter station footprint and 2) reduced costs and power losses.

This paper, based on the LCC HVDC system with controllable capacitors [1], tries to achieve 1) reductions of the required voltage rating and capacitance of controllable capacitors for CF elimination 2) while maintaining the AC voltage/reactive power control performance, and 3) satisfactory harmonic filtering performance without passive AC filters. It will be shown that by including additional fixed parallel capacitors at the valve side of converter transformer, these objectives can be achieved.

The rest of the paper is organized as follows. Section II introduces the proposed circuit configuration. Section III explains the commutation process of the proposed system, and presents the theoretical analysis of the system's harmonic performance. Section IV discusses the parameter selections of components. Section V firstly shows the simulation results of CF elimination performance of the proposed system and comparisons with the LCC HVDC system with controllable capacitors [1] are made. Secondly, AC voltage/reactive power control performance of the proposed system are illustrated and comparisons are made with LCC HVDC system with controllable capacitors [2]. Thirdly, the harmonic performance of the proposed system without AC filters is demonstrated and compared with conventional LCC HVDC systems with AC filters. Finally the voltage and current stress of the fixed parallel capacitors are shown and analyzed. Section VI concludes the paper.

## II. Circuit Configuration of the Proposed System

Fig. 1 shows the proposed circuit configuration and the connected AC system at inverter side. In the figure, $I_d$ is the DC current, $L_s$ is the DC smoothing reactor, *TY(D)1* to *TY(D)6* are thyristors valves, *LY(D)a*, *LY(D)b*, *LY(D)c* are current limiting inductors, *CapY(D)a*, *CapY(D)b*, *CapY(D)c* are controllable capacitors (each of which consists of a number of series connected capacitor submodules to achieve the required insertion voltage level), *CapY(D)ab*, *CapY(D)bc*, *CapY(D)ac* are fixed parallel capacitors and $Z_{inv}$ is the equivalent AC system impedance. The same insertion strategy of controllable capacitors as that described in [1] are applied. The whole system is based on the CIGRE benchmark model with all system parameters obtained from [24].

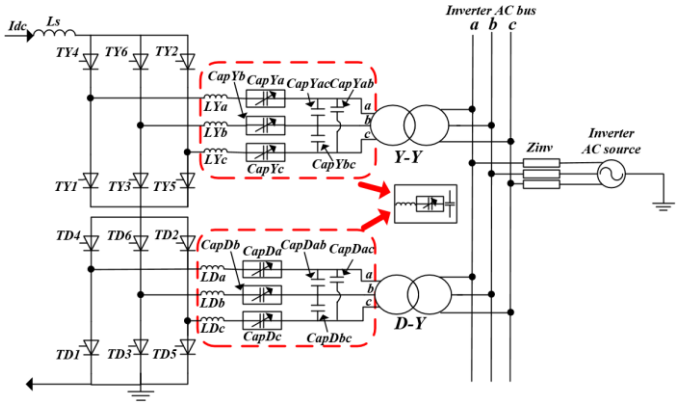



Fig. 1. Circuit configuration of the proposed system.

The main difference between the proposed system and the original LCC HVDC system with controllable capacitor [1] is that additional fixed parallel capacitors are connected between phases for each 6-pulse bridge. These parallel capacitors are located at the secondary side of converter transformer. By appropriate selection of the capacitor values, acceptable harmonic filtering performance can be achieved so that AC harmonic filters are not needed any longer on the AC system side in the proposed configuration (as shown in Fig. 1).

Another benefit brought by the fixed parallel capacitors is the increased speed of commutations. It is advantageous for

the success of commutations and directly leads to the following two benefits: 1) Significant reductions in the required voltage rating of the controllable capacitors; 2) Significant reductions in the required capacitance of the controllable capacitors.

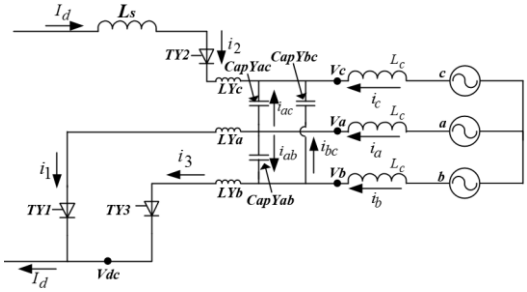
Both aspects are discussed in detail in section III. The current limiting inductors are generally small and are included to prevent excessively fast commutations. The parameter selections of parallel capacitors, current limiting reactors and controllable capacitors are presented in section IV.

## III. Effects of Fixed Parallel Capacitor on Commutation Process and Harmonic Filtering

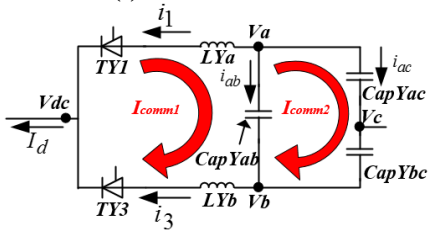
The fixed parallel capacitors affect two operational aspects of the 6-pulse bridge. The first is the speed of commutation, and the second is filtering of current harmonics. The analyses of these two aspects are presented in this section.

### A. Commutation Process

The commutation process of the proposed system can be physically understood with reference to Fig. 2, which shows the commutation from *TY1* to *TY3*. The insertion of controllable capacitor is not included as it is found that the extra commutation voltage from the controllable capacitors has less impact on the commutation speed than that from the parallel capacitors. Therefore for the sake of simplicity of the analysis, only the impact of the parallel capacitors on the commutation is considered in the following derivations while the impact of the controllable capacitors on the commutation is neglected. Fig. 2(a) shows the commutation circuit where $i_1$, $i_2$, $i_3$ are instantaneous currents through thyristors, $i_{ab}$, $i_{bc}$, $i_{ac}$ are the currents through parallel capacitors, $v_a$, $v_b$ and $v_c$ are three-phase voltages at the valve side of converter transformer, and $i_a$, $i_b$, $i_c$ are three-phase line currents. Fig 2(b) shows the equivalent circuit of the same commutation process where $I_{comm1}$ and $I_{comm2}$ are the commutation currents through parallel capacitors.




(a) Commutation circuit




(b) Equivalent commutation circuit

Fig. 2. Commutation from *TY1* to *TY3* of the proposed system.

Before the start of commutation, *TY3* is off and DC current is flowing through *TY2* and *TY1*, and there is no voltage across *LYa* and *LYb*. Once *TY3* is fired, the voltage of *Vdc* (shown in Fig. 2(a)) immediately changes to the average of $v_a$ and $v_b$ which is higher than $v_a$ and lower than $v_b$. It causes potential differences over *LYa* and *LYb*, driving current through them and forming the commutation current. This commutation current splits mainly between two paths, one through *CapYab* ($I_{comm1}$ as shown in Fig 2(b)) and the other one through *CapYac* & *CapYbc* ($I_{comm2}$ as shown in Fig 2(b)). Only a small amount of this commutation current flows into the network because the transformer inductance forms a high impedance path. As the rate of change of this commutation current is dependent on the size of *LYa* and *LYb*, the commutation can be made faster using smaller values of current limiting inductors. The rate of increase of $I_{comm1}$ is higher than that of $I_{comm2}$ as the capacitance of *CapYac* and *CapYbc* connected in series is smaller than the capacitance of *CapYab*.

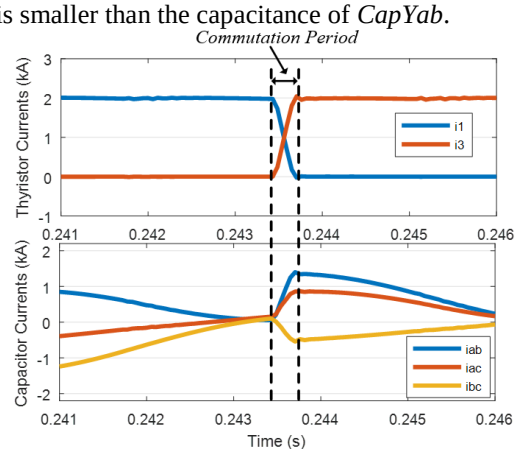



Fig. 3. Simulation results of commutation from *TY1* to *TY3*.

To better illustrate the process, Fig. 3 shows the simulation results of the same commutation process (from *TY1* to *TY3*). It can be seen from Fig. 3 that the commutation currents through the parallel capacitors are increased and drive down the current of $i_1$. The commutation process is completed once the sum of $i_{ab}$ and $i_{ac}$ is larger than the DC current. The negative value of $i_{bc}$ is due to the definition of the direction of current.

The following mathematical equations describing the commutation process will help the selection of parameters in Section IV. To be consistent but without losing generality, the same commutation process from *TY1* to *TY3* is considered. The instantaneous phase voltages are

$$\begin{aligned} e_a &= E_m \cos(\omega t + 60^0) \\ e_b &= E_m \cos(\omega t - 60^0) \\ e_c &= E_m \cos(\omega t - 180^0) \end{aligned} \quad (1)$$

where $E_m$ and $\omega$ are the phase voltage magnitude and AC system angular frequency, respectively. With firing angle $\alpha$, the fundamental frequency component of $i_a$ and $i_b$ will lag the corresponding phase voltages by approximately an angle of $\alpha$ [25]:

$$i_a = I_m \cos(\omega t + 60^0 - \alpha) \quad i_b = I_m \cos(\omega t - 60^0 - \alpha) \quad (2)$$

where $I_m$ is the current magnitude. This approximation is acceptable since the error caused by overlap is minimized with

a short commutation time. The relationships between currents in Fig. 2(a) can be written as

$$\begin{aligned} i_2 + i_{ac} + i_c + i_{bc} = 0 \qquad & i_1 + i_3 = I_d \\ i_1 + i_{ac} + i_{ab} = i_a \qquad & i_b + i_{ab} = i_3 + i_{bc} \end{aligned} \tag{3}$$

The currents through parallel capacitors are

$$i_{ab} = C\frac{d(v_a - v_b)}{dt} \quad i_{bc} = C\frac{d(v_b - v_c)}{dt} \quad i_{ac} = C\frac{d(v_a - v_c)}{dt} \tag{4}$$

where $C$ is the value of parallel capacitance. The voltages of $v_a$, $v_b$ and $v_c$ can be calculated by considering the voltage drop over $L_c$:

$$v_a = e_a - L_c\frac{di_a}{dt} \quad v_b = e_b - L_c\frac{di_b}{dt} \quad v_c = e_c - L_c\frac{di_c}{dt} \tag{5}$$

For commutation loop, the voltage equation can be written as

$$v_a - L\frac{di_1}{dt} = v_b - L\frac{di_3}{dt} \tag{6}$$

where $L$ is the inductance of current limiting inductor. By combining equations (1) and (3)-(5), the following differential equation for $i_1$ can be obtained:

$$\frac{di_1^3}{dt^3} + \left(\frac{1}{3L_cC} + \frac{1}{3LC}\right)\frac{di_1}{dt} + \frac{\sqrt{3}E_m \sin\omega t}{6LL_cC} = 0 \tag{7}$$

The initial conditions are

$$i_1\big|_{t=\alpha/\omega} = I_d \tag{8}$$

$$\left.\frac{di_1}{dt}\right|_{t=\alpha/\omega} = \left.\frac{v_a - v_b}{2L}\right|_{t=\alpha/\omega} = \frac{-\sqrt{3}E_m \sin\alpha + \sqrt{3}L_c I_m \omega}{2L} \tag{9}$$

$$\left.\frac{di_1^2}{dt}\right|_{t=\alpha/\omega} = \frac{1}{2L}\left.\frac{d(v_a - v_b)}{dt}\right|_{t=\alpha/\omega} = \frac{-\sqrt{3}E_m \omega\cos\alpha}{2L} \tag{10}$$

The expression of $v_a$ and $v_b$ in (9) and (10) are obtained by substituting (2) into (5). With the calculated initial conditions, solution for (7) can be found:

$$i_1 = C_1 + C_2\cos\sqrt{a}t + C_3\sin\sqrt{a}t - \frac{b}{\omega^3 - a\omega}\cos\omega t \tag{11}$$

where

$$\begin{aligned} a &= \frac{1}{3L_cC} + \frac{1}{3LC} \quad b = \frac{\sqrt{3}E_m}{6L_cLC} \quad B = \sin\sqrt{a}\frac{\alpha}{\omega} \quad D = \cos\sqrt{a}\frac{\alpha}{\omega} \\ C_1 &= -\frac{b}{a\omega}\cos\alpha + I_d - \frac{\sqrt{3}E_m\omega\cos\alpha}{2La} \\ C_2 &= \left(\frac{\sqrt{3}E_m}{2L} + \frac{b}{\omega^2 - a}\right)\left(\frac{B\sin\alpha}{\sqrt{a}} + \frac{D\omega\cos\alpha}{a}\right) - \frac{\sqrt{3}BI_mL_c\omega}{2L\sqrt{a}} \\ C_3 &= \left(\frac{\sqrt{3}E_m}{2L} + \frac{b}{\omega^2 - a}\right)\left(\frac{\omega\cos\alpha}{aB} - \frac{D\sin\alpha}{\sqrt{a}} - \frac{D^2\omega\cos\alpha}{aB}\right) + \frac{\sqrt{3}DI_mL_c\omega}{2L\sqrt{a}} \end{aligned} \tag{12}$$

### *B. Harmonic Filtering*

The 6-pulse bridge can be approximated by a harmonic current source on the AC side [3]. To analyze the harmonic filtering performance of the proposed system, the level of harmonic current that enters into the network is to be evaluated. The Harmonic Factor (HF), i.e., the percentage of individual harmonic magnitude over the fundamental component, is calculated in this section. The Total Harmonic Distortion (THD) for both AC voltages and currents are presented in Section V.

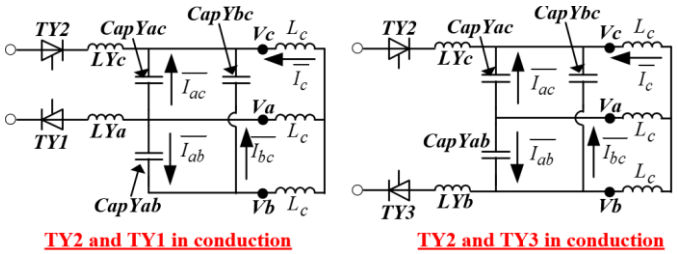



Fig. 4. Conduction circuits when *TY2* is conducting.

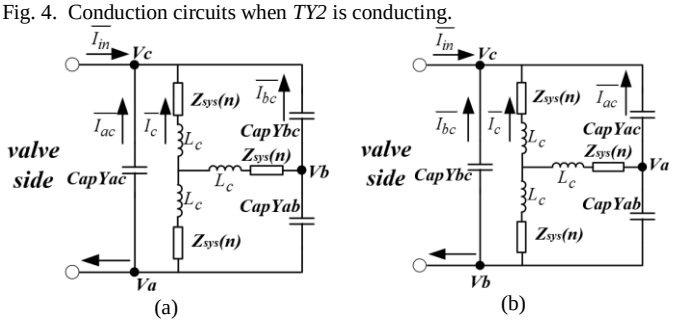



Fig. 5. Equivalent circuits. (a) *TY1* and *TY2* are conducting; (b) *TY2* and *TY3* are conducting.

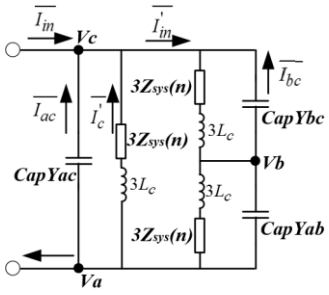



Fig. 6. Equivalent circuit after transformation.

Due to the symmetry of operation of the 6-pulse bridge, the harmonic performance of each phase is the same. Therefore for the simplicity of analysis, phase C is considered in the following calculations. Further noticing that the harmonic equivalent circuit is the same when either *TY2* or *TY5* is conducting, the operation of half a cycle of phase *C* current is considered (i.e., when *TY2* is in conduction). Fig. 4 shows the conduction paths when *TY2* is conducting and Fig. 5 shows the corresponding equivalent circuits. In Fig. 4 and Fig. 5, $\overline{I_{ab}}$, $\overline{I_{bc}}$, $\overline{I_{ac}}$, $\overline{I_c}$, $\overline{I_{in}}$ are the phasor values of currents, and in Fig. 5 $Z_{sys}(n)$ represents the network impedance at $n^{th}$ harmonic frequency. By observing Fig. 5(a) and Fig. 5(b), it can be seen that although circuit topologies are different due to commutation, the harmonic current that enters into the network for phase *C* (i.e. $\overline{I_c}$) are the same under the same harmonic current injection from converter ($\overline{I_{in}}$). Therefore, Fig. 5(a) will be used for the following calculations.

Fig. 6 shows the equivalent circuit by performing delta-star transformation to Fig. 5(a). The circuit equations of Fig. 6 are

$$\overline{I_{ac}} \times \frac{1}{jn\omega C} = \overline{I_c'} \times \left(3jn\omega L_c + 3Z_{sys}(n)\right) \tag{13}$$

$$-\overline{I_{bc}} \times \frac{1}{jn\omega C} = \left(\overline{I_{in}'} + \overline{I_{bc}}\right) \times \left(3jn\omega L_c + 3Z_{sys}(n)\right) \tag{14}$$

$$\overline{I_c} = -\overline{I_{in}} - \overline{I_{ac}} - \overline{I_{bc}} \tag{15}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPWRS.2018.2800666, IEEE Transactions on Power Systems



$$\overline{I_{ac}} \times \frac{1}{jn\omega C} == -\overline{I_{in}^{'}} \times 2 \times \frac{\left(3jn\omega L_c + 3Z_{sys}(n)\right) \times 1/jn\omega C}{\left(3jn\omega L_c + 3Z_{sys}(n)\right) + 1/jn\omega C} \quad (16)$$

$$\overline{I_{in}} + \overline{I_{ac}} + \overline{I_c^{'}} = \overline{I_{in}^{'}} \quad (17)$$

According to (13)-(17), the harmonic current of phase *C* that enters into the network is calculated as

$$\overline{I_c} = \frac{-1}{\left(3jn\omega L_c + 3Z_{sys}(n)\right) \times jn\omega C + 1} \overline{I_{in}} \quad (18)$$

The harmonic voltage can then calculated as

$$\overline{V_{sys\_n}} = 2 \times \frac{-Z_{sys}(n)}{\left(3jn\omega L_c + 3Z_{sys}(n)\right) \times jn\omega C + 1} \overline{I_{in}} \quad (19)$$

For 12-pulse configuration, the total harmonic current injection is two times of that for each 6-pulse. (18) and (19) are used in Section IV for the selection of parallel capacitance.

## IV. Parameter Selection for Components

In the proposed system, two component parameters need to be selected: 1) capacitance of the fixed parallel capacitors and 2) inductance of the current limiting inductors. Capacitance is selected so that the harmonic limits are met, and the inductance is selected so that the speed of commutation is sufficiently fast but still within acceptable/safe range. In addition, with the improved performance of the proposed system, the required voltage rating and capacitance value of controllable capacitors need to be determined.

### *A. Selection of Capacitance*

#### *1) Harmonic Number*

The harmonic current generated by an ideal 6-pulse bridge can be expressed using Fourier series:

$$i_{in} = \frac{2\sqrt{3}I_d}{\pi}\left(\sin\omega t - \frac{1}{5}\sin 5\omega t - \frac{1}{7}\sin 7\omega t - \frac{1}{11}\sin 11\omega t + \ldots\right) \quad (20)$$

As the 5th and 7th harmonics are effectively cancelled by the 12-pulse configuration, the filtering performances for 11th and higher order harmonics are considered for the selection of capacitance.

#### *2) AC Network Impedance*

From (18) it can be seen that the harmonic impedance of the network, which can change dramatically with the change of operating condition or circuit configuration, affects the filtering performance. Normally the network harmonic impedance is predominantly inductive around the 11th harmonic frequency and this contributes positively to the filtering performance according to (18). If the harmonic impedance is capacitive around the 11th harmonic frequency, for example for networks with significant shunt capacitance, the filtering performance is decreased. The worst case scenario is that when the capacitive impedance of the network effectively cancels out the inductive impedance of converter transformer at the considered frequency. In this case the combined impedance of $\left(3jn\omega L_c + 3Z_{sys}(n)\right)$ is resistive, the value of which depends on the resistive component of the network impedance at harmonic frequency. So a larger value of capacitance may be needed to provide acceptable filtering performance. At harmonic orders of 23rd or higher, the network harmonic impedance can be either inductive or capacitive depending on system conditions. If it is inductive, as discussed, it contributes positively to the filtering. If it is capacitive, the combined impedance of $\left(3jn\omega L_c + 3Z_{sys}(n)\right)$ will still has a relatively large magnitude and results in acceptable filtering performance. This is because the magnitude of network impedance will be decreased at higher frequencies, while the equivalent impedance of converter transformer $3jn\omega L_c$ is increased with increased frequencies.

To limit the level of harmonic distortion in practical project, harmonic impedance of the connected AC system under all probable operating conditions need to be considered for both present and future conditions. Uncertainties in system parameters should also be considered. Then analysis needs to be carried out to determine the range of required capacitances so that the harmonics are within the specified limits at the point of common coupling. Normally smaller capacitance within the desired range is preferred to reduce the investment cost. As the insertion of controllable capacitors have small impact on the harmonic generation of converter [1], the harmonic filtering performance with the obtained parallel capacitance will not be compromised.

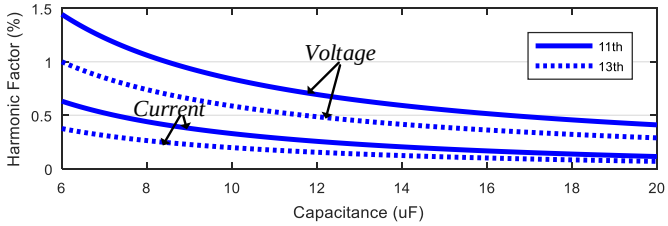



Fig. 7. HF for different values of parallel capacitance.

In this paper, for the purpose of demonstration, parameters of the CIGRE benchmark model are used to calculate the HF of voltage and current for 11th and 13th harmonics. The calculation results are shown in Fig. 7. From Fig. 7 it can be seen that the filtering is better for 13th harmonic frequency, hence the selection of capacitance is based on the filtering performance of 11th harmonic frequency. According to [26], the harmonic current and voltage limits for 11th harmonic order are 0.5% and 1% respectively. So by observing Fig. 7, the capacitance value of 10μF is selected to meet the harmonic limits.

#### *3) Non-Characteristic Harmonics*

For practical projects, the ideal assumptions made in theoretical studies cannot be fulfilled in reality. As a consequence, harmonics of orders other than the characteristic ones will appear i.e., non-characteristic harmonics. These harmonics are normally of much lower magnitude than the characteristic harmonics [6], and the uncertain nature of the non-characteristic harmonics makes it difficult to prevent them at the design stage [27]. These non-characteristic harmonics can be problematic when resonance condition exists between the AC filter banks and the system impedance at these harmonic orders [28].

The main reasons for the generation of non-characteristic harmonics are [28]: 1) Unbalance of AC system voltage; 2) Unbalance of converter transformers and 3) Firing angle asymmetry. Simulation studies are presented in Section V considering these categories to show the filtering performance of the proposed method. Comparisons are made with benchmark system.

### B. Selection of Current Limiting Inductor

According to (11), at the end of commutation,

$$i_1(\alpha+\mu)=0 \tag{21}$$

where $\mu$ is the overlap angle. With the selected value of capacitance, (21) can be used to solve $\mu$ for different values of $L$. Fig. 8 shows the calculation results. It can be seen that the overlap angle is much smaller compared with conventional LCC HVDC system (normally higher than 20 degrees). This increased speed of commutation results in a lower capacitor voltage rating for CF elimination. However, the speed cannot be made arbitrarily fast because an excessively high rate of current rise can cause thermal breakdown of the thyristor [6]. Maximum rate of current rise is normally in the range of 200-300A/μs, and for safe operation of thyristors, the rate of current rise must be limited to be significantly lower [6]. For commutation from *TY1* to *TY3* as discussed in previous section, the highest rate of current rise for $i_3$ takes place at the start of commutation, i.e.,

$$\left.\frac{di_3}{dt}\right|_{t=\alpha/\omega} = -\left.\frac{di_1}{dt}\right|_{t=\alpha/\omega} = \frac{\sqrt{3}E_m\sin\alpha-\sqrt{3}L_cI_m\omega}{2L} \tag{22}$$

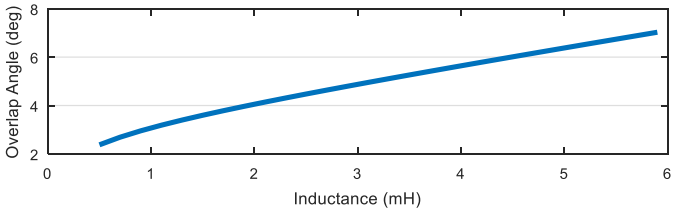



Fig. 8. Overlap angle for different values of current limiting inductor.

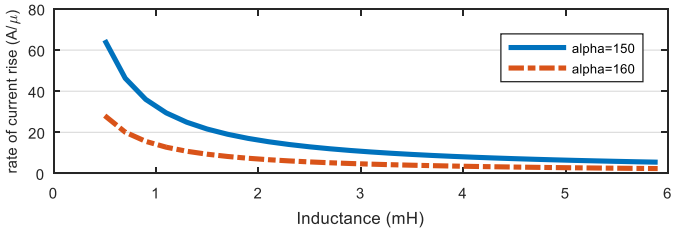



Fig. 9. Rate of current rise for different values of current limiting inductor.

Fig. 9 shows the highest rate of current rise for different values of $L$ at two different values of firing angles according to (22). From Fig. 9 it is observed that the rate of current rise is generally much lower than 100A/μs, and is higher for smaller values of firing angle. Considering both the speed of commutation and the limit on the rate of current rise, the inductance value of 2mH is selected for the current limiting inductor. This corresponds to an overlap angle of about 4 degrees and a rate of current rise of less than 20A/μs.

### C. Voltage Rating of Controllable Capacitors

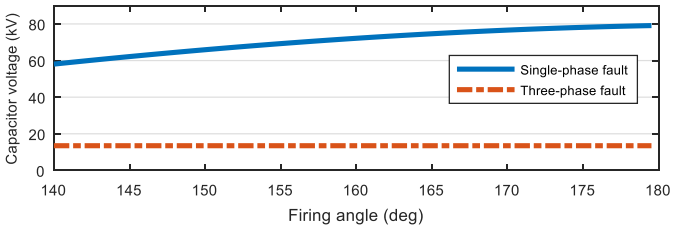



Fig. 10. Required insertion voltage level for single-phase and three-phase fault.

Using the calculation method from [1] but with a reduced overlap angle, the required insertion voltage level of controllable capacitor in the proposed system can be calculated for single-phase fault and three-phase fault (Fig. 10). The required voltage level for single-phase fault is higher than that for three-phase fault, but is significantly lower than that for the LCC HVDC system with controllable capacitor (140kV) [1]. Considering a normal inverter firing angle between 140 to 155 degrees, the voltage reference for controllable capacitors in the proposed system is chosen to be 70kV, which is half of the voltage rating required in the LCC HVDC system with controllable capacitors. As the voltage level for each capacitor submodule is limited by the voltage rating of power electronic switches to a few kV, the number of required capacitor submodule to achieve the total level of voltage insertion is therefore significant reduced. This then directly results in significant reductions of investment cost and power losses as a smaller number of power electronic switches is required.

### D. Capacitance of Controllable Capacitors

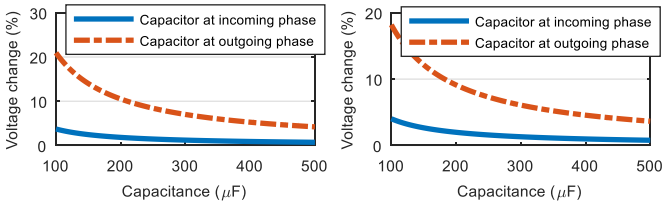



Fig. 11. Percentage of voltage change of controllable capacitors. (a) Three-phase fault; (b) Single-phase fault.

With a smaller commutation overlap angle in the proposed system, the level of voltage change of controllable capacitor for each commutation is reduced. This permits the use of a smaller capacitance. Using the calculation method in [1], Fig. 11 shows the percentage of voltage change of controllable capacitor under three-phase fault and single-phase fault. Based on Fig. 11, if a maximum 10% voltage variation is chosen then the capacitance is selected to be 225μF. This is more than 60% reduction compared with the capacitance selected for LCC HVDC system with controllable capacitors (585 μF) [1]. In terms of implementation, 24 capacitor submodules are required considering the voltage level of 3kV for each submodule (70kV insertion level). Therefore the capacitance for each submodule will be 225μF×24=5400μF, which is similar to the value of capacitances used for Modular Multilevel Converter (MMC) (normally at least a few thousand micro Farads (μF) and up to ten thousand μF [29]).

The advantage of this reduction in capacitance compared with the original development in [1] is that the size of capacitor in each submodule is significantly reduced. Consider that the submodule capacitor accounts for over 50% of the total size and 80% of the weight of each submodule [30], smaller capacitance directly leads to smaller physical size, less weight and also less investment cost.

## V. Simulation Results

### A. Commutation Failure Elimination

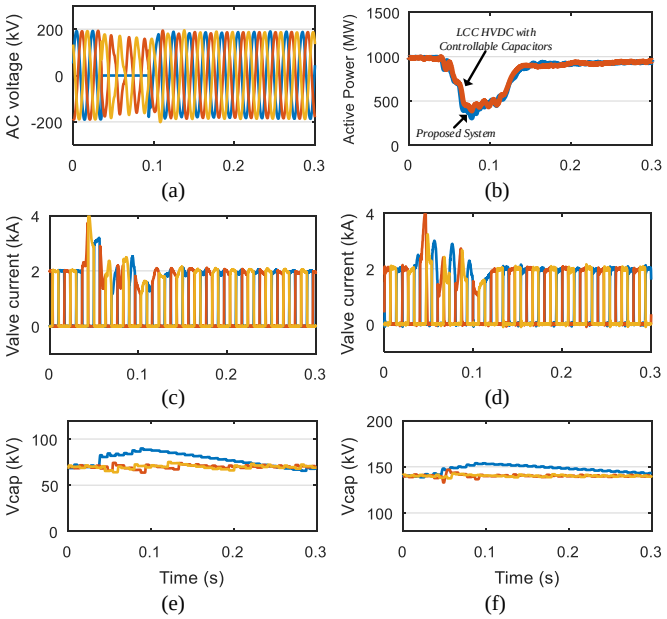



Fig. 12. Performance of commutation failure elimination. (a) AC voltage; (b) Active power; (c) Valve currents of the proposed system; (d) Valve currents of the LCC HVDC system with controllable capacitor; (e) Capacitor voltages of the proposed system; (f) capacitor voltages of the LCC HVDC system with controllable capacitor.

As illustrated in last section, elimination of CF for single-phase fault requires higher voltage insertion than three-phase fault. Therefore to demonstrate the performance of CF elimination using the proposed method, zero impedance single-phase fault is simulated for comparison. As discussed in Section IV a voltage insertion level of 70kV is implemented in the proposed method. Simulation results of a 50ms zero impedance single-phase fault are shown in Fig. 12. During the fault phase A voltage drops to zero (Fig. 12(a)), but no CF is observed in both systems as shown in Fig. 12(c) and Fig. 12(d). As a result, the proposed system is able to transmit active power during the fault (Fig. 12(b)), similar to that of the LCC HVDC system with controllable capacitors [1]. As demonstrated by Fig. 12(e), although the size of capacitor is significantly reduced in the proposed method, the capacitor voltages are satisfactorily controlled.

### B. Power System Dynamic Performance

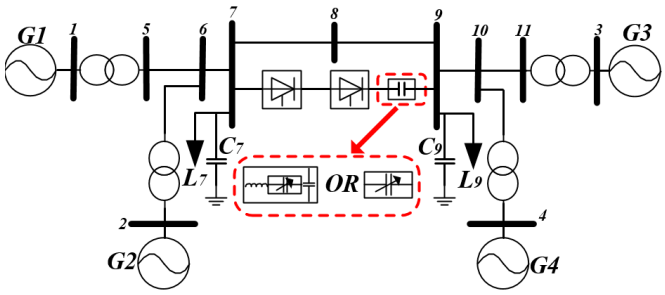



Fig. 13. Test power systems.

To demonstrate the effectiveness of the proposed method in improving power system dynamic performance, the four-machine two-area power system with the proposed system is simulated in RTDS. As shown in Fig. 13, one of the transmission lines between bus 7 and bus 9 is replaced with the proposed system or the LCC HVDC system with controllable capacitors. The load level is adjusted so that in both cases the HVDC link is transmitting 1000MW under steady-state. For both HVDC systems, the rectifier is controlling the active power, and the inverter is controlling the AC voltage.

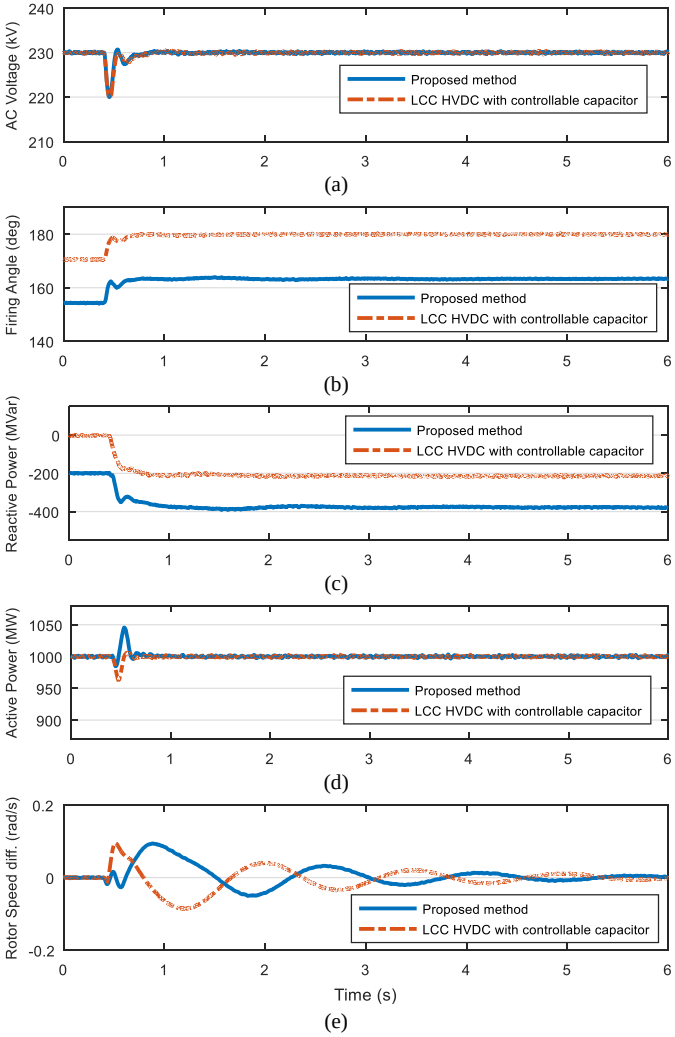



Fig. 14. Power system dynamic performance with the proposed method. (a) Bus 9 AC voltage; (b) Inverter firing angle; (c) Inverter reactive power consumption; (d) DC power; (e) Rotor speed difference between G2 and G4.

Under steady-state condition, the inverter side controller of both HVDC systems are controlling the AC voltage of bus 9 to be at rated values (shown in Fig. 14(a)). The reactive power consumption at inverter side of the LCC HVDC system with controllable capacitors [2] is zero, while the reactive power consumption of the proposed system is negative as shown in Fig. 14(c). The negative sign indicates that the proposed system is exporting reactive power into the AC system, unlike traditional LCC HVDC system which absorbs reactive power. This is because with the selected parallel capacitance, the reactive power provided from the parallel capacitors exceeds the reactive power requirement of the inverter. It needs to be mentioned that the contribution of reactive power from the controllable capacitors is limited as they are mainly inserted during the commutation periods to eliminate CF.

For practical LCC HVDC systems, there is always some reactive power exchange with the connected AC system [6]. The important design criterion is to ensure that the level of reactive power exchange remains within the specified limits [6, 8]. This is to make sure that the AC bus voltage is within the operating limits and the transmission capability of AC line is not limited by excessive level of reactive power exchange.

For AC systems with relatively wide range of permitted reactive power exchange, the reactive power export with the proposed method is acceptable. For AC systems with stringent reactive power exchange limit, two measures can be adopted [8]: 1) installation of shunt reactors or 2) design the HVDC converters to operate at higher extinction angles. These measures can help ensure that the reactive power exchange limits are not violated in the whole active power range. The installation of shunt reactor will lead to additional cost and land requirement but at much lower level compared to the savings from the elimination of AC filters. The operation with higher extinction angle will increase the number of thyristors and the protection level [8]. Therefore the actual implementation of any one or both of the measures will require a detailed techno-economic analysis based on the operational requirements and constraints of the HVDC project.

At 0.5s, reactive load at bus 9 is increased by 200MVar. The inverter side controllers of both systems react to increase the level reactive power export, as shown in Fig. 14(b) and Fig. 14(c). As a result, the AC voltage at bus 9 is brought back to the rated value, which is shown in Fig. 14(a). It can be seen from Fig. 14(d) that once reactive load changes, the DC active power of the proposed system is increased while it is decreased for the LCC HVDC system with controllable capacitors. It is because for the proposed system, the increased inverter firing angle causes an increase of DC voltage, which results in an increase of DC power. For the LCC HVDC system with controllable capacitors, considering overlap angle, the commutation completes after the commutation voltage becomes negative. Then an increase of firing angle causes a decrease of DC voltage, and subsequently a decrease of DC power. Considering that the increase of reactive power load is normally accompanied with the increase of active power load, this increase of transmitted DC active power is beneficial to balance the increased active power demand. This change of DC power leads to different changes of rotor speed difference as illustrated in Fig. 14(e). From Fig. 14(e), it can also be observed that similar damping performance is achieved with the proposed system.

### C. Filtering Performance of Characteristic Harmonics

To verify the harmonic filtering performance of the proposed system without AC filters, simulation results are presented together with the calculated HF and THD. Comparisons are made with the benchmark system with AC filters. Fig. 15 shows the simulation results of one 6-pulse bridge for the proposed system. It can be seen that the square wave current from the 6-pulse bridge (Fig. 15(a)) is effectively filtered by the parallel capacitors (Fig. 15(b)). The current after filtering is shown in Fig. 15(c), where the main harmonics are of 5$^{th}$ and 7$^{th}$ order. Fig. 15(d) shows the total injected AC current from the 12-pulse bridge into the AC network. Table I further shows the values of HF for the waveforms in Fig. 15. From Table I it can be seen that the values of HF for 11$^{th}$ and 13$^{th}$ harmonic currents are both within limits, as expected from theoretical analysis in Section IV.

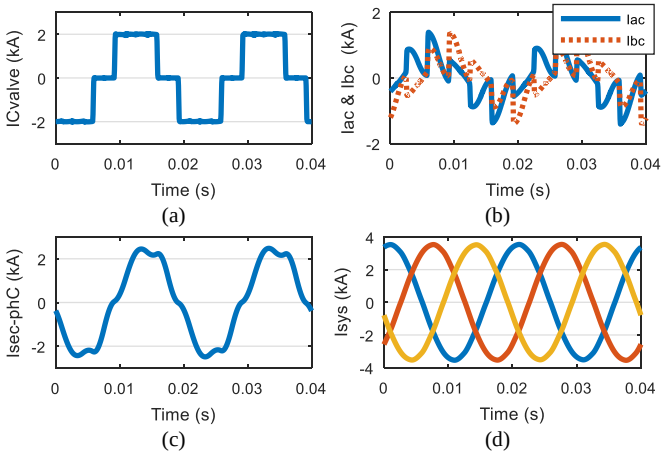



Fig. 15. Electrical variables of the proposed system. (a) Phase *C* current; (b) $I_{ac}$ and $I_{bc}$; (c) Phase *C* current at secondary side of converter transformer; (d) Injected AC network current.

TABLE I
HF FOR PROPOSED SYSTEM

| n | *ICvalve* | $I_{ac}$ & $I_{bc}$ | *Isec-phC* | *Isys* |
|---|---|---|---|---|
| 5$^{th}$ | 19.88% | 17.6% | 9.53% | 0.15% |
| 7$^{th}$ | 14.24% | 9.97% | 2.74% | 0.07% |
| 11$^{th}$ | 9.08% | 5.48% | 0.33% | 0.33% |
| 13$^{th}$ | 7.33% | 4.33% | 0.18% | 0.18% |

TABLE II
COMPARISON BETWEEN PROPOSED AND BENCHMARK SYSTEMS

| n | IEEE Limits (V/I) | | Proposed System | | Benchmark System | |
|---|---|---|---|---|---|---|
| | V (%) | I (%) | V (%) | I (%) | V (%) | I (%) |
| 11$^{th}$ | 1% | 0.5% | 0.83% | 0.33% | 0.68% | 0.28% |
| 13$^{th}$ | 1% | 0.5% | 0.55% | 0.18% | 0.48% | 0.17% |
| 23$^{rd}$ | 1% | 0.15% | 0.18% | 0.04% | 0.37% | 0.07% |
| 25$^{th}$ | 1% | 0.15% | 0.15% | 0.03% | 0.30% | 0.05% |
| THD | 1.5% | 1.5% | 1.05% | 0.51% | 0.96% | 0.52% |

Table II shows the comparison of HF and THD for both AC voltage and current between the proposed system and the benchmark system. Recommended harmonic limits for voltage and current from [26] are also included in the table. It can be

seen from Table II that HF and THD for voltage and current in the proposed system are within recommended limits. The values of HFs are higher for 11th and 13th harmonics in the proposed system than benchmark system, and lower for higher order harmonics. The THDs for both voltage and current are similar between the proposed system and benchmark system. If better harmonic performance is desired, higher capacitance can be used.

### *D. Filtering Performance of Non-Characteristic Harmonics*

TABLE III
HARMONIC COMPARISON FOR CASE 1

| n | Proposed System | | Benchmark System | |
|---|---|---|---|---|
| | V (%) | I (%) | V (%) | I (%) |
| 1st | 100% | 100% | 100% | 100% |
| 3rd | 0.35% | 0.41% | 0.38% | 0.49% |
| 9th | 0.0065% | 0.0033% | 0.051% | 0.027% |

TABLE IV
HARMONIC COMPARISON FOR CASE 2

| n | Proposed System | | Benchmark System | |
|---|---|---|---|---|
| | V (%) | I (%) | V (%) | I (%) |
| 1st | 100% | 100% | 100% | 100% |
| 3rd | 0.08% | 0.07% | 0.18% | 0.05% |
| 5th | 0.12% | 0.16% | 0.22% | 0.16% |
| 7th | 0.13% | 0.069% | 0.17% | 0.073% |
| 9th | 0.0025% | 0.0017% | 0.03% | 0.0017% |

TABLE V
HARMONIC COMPARISON FOR CASE 3

| n | Proposed System | | Benchmark System | |
|---|---|---|---|---|
| | V (%) | I (%) | V (%) | I (%) |
| 1st | 100% | 100% | 100% | 100% |
| 2nd | 0.045% | 0.07% | 0.045% | 0.054% |
| 3rd | 0.01% | 0.09% | 0.01% | 0.02% |
| 4th | 0.0094% | 0.0055% | 0.018% | 0.022% |
| 5th | 0.18% | 0.14% | 0.33% | 0.26% |
| 6th | 0.0028% | 0.0024% | 0.0035% | 0.0028% |
| 7th | 0.11% | 0.07% | 0.17% | 0.097% |
| 8th | 0.0022% | 0.0023% | 0.0009% | 0.0006% |
| 9th | 0.0012% | 0.0014% | 0.0013% | 0.00085% |
| 10th | 0.0012% | 0.0007% | 0.0013% | 0.0011% |

To show the harmonic filtering performance of non-characteristic harmonics with the proposed method, the following three case studies have been carried out (similar to tests carried out in [28]) and comparisons have been made with the benchmark system:

Case 1: The voltage in one phase (phase A) is reduced by 1% with respect to the other two.

Case 2: The transformer leakage reactance is 19% in one phase and 18% for the rest five phases.

Case 3: The firing angle is delayed by 1 degree in one of the valves while the firing angles for other valves are intact.

Table III, Table IV and Table V show the simulation results for Case 1, Case 2 and Case 3, respectively. The results for harmonic orders between 2 to 10 are listed [28].

For Case 1, the voltage unbalance produces harmonics by its influence on the firing angle and the overlap angle in different phases. It will result in harmonics of order $n=k\times p\pm 3$ (where $k$=0, 1, 2, … $p$= converter pulse number) [6]. It can be seen from Table III that harmonic magnitudes are small for both the proposed system and benchmark system and better harmonic filtering is achieved with the proposed method.

For Case 2, the reactance imbalance between phases is a result of manufacturing tolerances and can be of the order of 1% [28]. It generates harmonics of the orders of 3, 5, 7, 9, … [28]. It can be seen from Table IV that the harmonic magnitudes are small and better filtering performance of the proposed method is obtained for most of the harmonic orders (with only slightly higher 3rd harmonic current for the proposed method).

For Case 3, the deviation in firing angle between the valves is caused primarily by variations in the delay of firing pulse between the control system and valves. It is usual to consider a valve firing accuracy within ±0.2 degree [28] but a value of 1 degree is used in the simulation study due to the limitation from simulation time-step. The firing angle asymmetry gives rise to harmonics of all orders and the results are shown in Table V. It can be seen from the table that again the filtering performance of the proposed method is better than the benchmark system.

For practical projects extensive simulation studies using detailed network impedance under various operating conditions (for both present and future network conditions) should be carried out to identify potential low order harmonic resonances. If there is a risk of low order resonance at non-characteristic harmonic frequencies, two possible methods can be taken: 1) limit the non-characteristic harmonic currents by having smaller tolerances on transformer reactance, transposition of lines, etc. [28] or 2) install additional filter to modify the AC side impedance to detune the resonance or limit the magnification of resonance to an acceptable value.

### *E. Dynamics of Controllable Capacitor*

Fig. 16 shows the switching waveforms of controllable capacitor in phase C (*CapYc* shown in Fig. 1). The four plots on the left (Fig. 16(a), Fig. 16(c), Fig. 16(e) and Fig. 16(g)) show the phase C current (before parallel capacitor), capacitor current of *CapYc*, switching pulses of *CapYc* and capacitor voltage of *CapYc* respectively in the proposed system where the parallel capacitor is installed. The other four plots on the right (Fig. 16(b), Fig. 16(d), Fig. 16(f) and Fig. 16(h)) show the same electrical variables for system without parallel capacitor (with insertion voltage level of 140kV from controllable capacitor) [1]. In Fig. 16, $t_1$ is the time instant when *CapYc* is inserted for charging and $t_2$, $t_3$, $t_4$, $t_5$ are the time instants of the start of commutations from *TY2* to *TY4*, *TY3* to *TY5*, *TY5* to *TY1*, *TY6* to *TY2*, respectively. As the capacitor voltage is lower than the reference, it is inserted ($t_1$) before the start of commutation from *TY2* to *TY4* ($t_2$). The positive direction of phase C current is defined as flowing into the converter. The positive switching pulse means that the positive polarity of the controllable capacitor is facing the valve side when inserted. It can be seen from Fig. 16(a) to Fig. 16(d) that none zero current is flowing through the controllable capacitor mainly during commutation periods. This is because the controllable capacitor is mainly inserted into the circuit during commutation periods [1] (Fig. 16(e) and Fig. 16(f)). In addition it can be seen that the capacitor current

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPWRS.2018.2800666, IEEE Transactions on Power Systems



charges the capacitor when the thyristor valves connected to phase C (*TY2* and *TY5* in Fig. 1) are switching out, and discharges the capacitor when *TY2* and *TY5* are switching in.

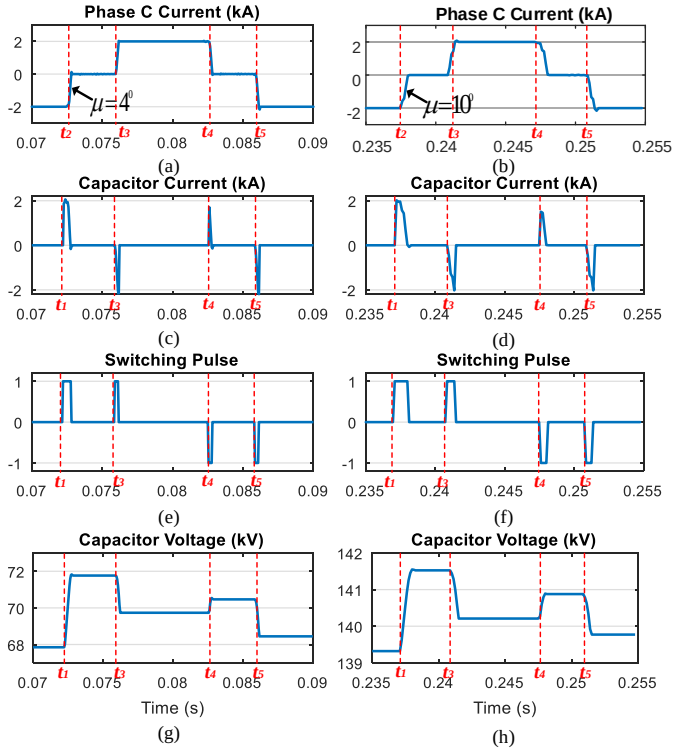



Fig. 16. Switching waveforms of the controllable capacitor *CapYc* in the proposed method and the method without parallel capacitor.

The main impact of parallel capacitor on the operation of controllable capacitor is the reduction of commutation overlap angle $\mu$ (discussed in Section III) as highlighted in Fig. 16(a) and Fig. 16(b). This reduction of overlap angle leads to a smaller current-time area of capacitor currents during commutation periods (Fig. 16(c) and Fig. 16(d)), therefore reduces the level of charging/discharging. So when parallel capacitor is installed, smaller capacitance can be used (as discussed in Section IV). As a result of using smaller capacitance, the level of capacitor voltage change during commutation is increased (Fig. 16(g) and Fig. 16(h)).

### *F. Voltage & Current Stress of the Fixed Parallel Capacitors*

The voltage and current stress of parallel capacitors are examined under both steady-state and transient conditions. Zero impedance single-phase fault and three-phase fault are simulated. Fig. 17(c) and Fig. 17(d) show the voltage across and current through parallel capacitors during single-phase fault. As fault happens, the peak value of capacitor voltage reaches about 1.48 times of that in steady-state (Fig. 17(a)). The peak value of capacitor current reaches 1.7 times of that in steady-state. Fig. 17(e) and Fig. 17(f) show the simulation results for three-phase fault. The transient peak voltage is 1.14 times the steady-state value, and transient peak current is 1.73 times the steady-state value. For fault cases with non-zero fault impedance, which most of the faults do, the peak values of both transient voltage and current of capacitors are lower.

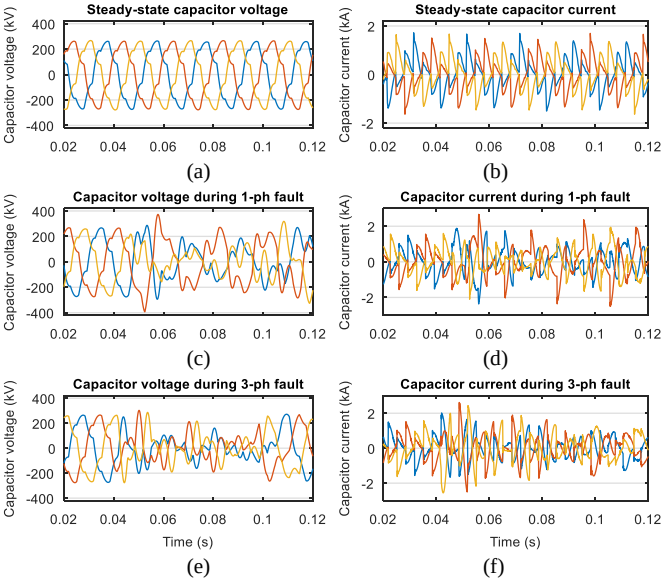



Fig. 17. Voltage and current stress of parallel capacitors under steady-state and transient conditions.

### *G. Practical Implementation*

To further justify the practical application of the proposed method, a comparison in terms of the physical implementation and the control strategy is made between the proposed method and the MMC converter.

*Number of Capacitor Submodules:* For physical implementation, a comparison of the required number of capacitor submodules is made between the proposed method and a 500kV MMC converter, as the number of capacitor submodule directly determines the complexity of practical implementation. For the proposed method, with a voltage insertion of 70kV in each phase the number of required submodules is $70/V_{cn}$ for each phase (where $V_{cn}$ is the submodule capacitor voltage) and $6\times70/V_{cn}$ for the whole 12-pulse system. For the 500kV MMC converter, the number of submodule in each arm is $500/V_{cn}$ and $6\times500/V_{cn}$ for the whole converter. Thus the required number of capacitor submodules of the proposed method is about 70/500=14% of that of the MMC converter valves, which also means a much lower complexity in practical implementation due to small number of capacitor submodules in comparison to that of a MMC converter.

*Control Complexity*: In terms of control strategy, the control of the capacitor submodules in the proposed method is decoupled from the main controller of LCC inverter, and these capacitor submodules are controlled independently from each other [1]. Each submodule capacitor voltage is naturally balanced due to the "push" and "pull" insertion strategy and hence only simple balancing strategy (as detailed in Subsection C of Section III in [1]) is required [1] without the need for coordination between submodule controls and complex sorting algorithms for MMC converter as presented in [31]. On the contrary for MMC converters, detailed coordination and complex sorting algorithms are required for the large number of submodules in each arm for the purpose of capacitor voltage balancing, which leads to challenging

requirements on both the speed and accuracy of control systems. Moreover, other control functions for example to suppress second harmonic circulating current and to improve converter performance under unbalanced grid conditions are normally required to be implemented in MMC converter. These control functions are not required in the proposed method.

Therefore it can be seen that the complexity in physical implementation and control strategy of the proposed method are significantly lower than that of a MMC converter. Together with the significant improvement in performance in terms of CF elimination, elimination of passive AC filters, and reduction of converter station footprint, the proposed method is potentially justifiable for practical applications.

## VI. Conclusion

This paper has proposed an AC filterless Flexible LCC HVDC system with fixed parallel capacitors at secondary side of converter transformer. It has been shown both mathematically and through simulation results that the harmonic limits can be met without the installation of AC filters. This directly leads to significant reduction of converter station footprint. Costs and losses associated with AC filters are also eliminated. At the same time, up to 50% reduction in voltage rating and more than 60% reduction in the capacitance of controllable capacitors have been achieved while similar performances in CF elimination and AC voltage/reactive power control as those in LCC HVDC system with controllable capacitors [1, 2] are maintained. The voltage/current stress of parallel capacitors under severe fault conditions has been analyzed and no significant overvoltage or overcurrent is observed.

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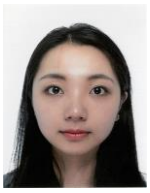

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